KL

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/513,067	02/24/2000	Christopher J. De Simmone	AB-928 US	5695

24251 7590 04/08/2002

SKJERVEN MORRILL MACPHERSON LLP
25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110

EXAMINER
LUU, CHUONG A

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/513,067	DE SIMMONE ET AL.	
	Examiner	Art Unit	
	Chuong A Luu	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3, 6-7, 10-14, and 16-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *37-43* is/are allowed.

6)☒ Claim(s) *1-3, 6-7, 10-14, and 16-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *7* .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Since this application is eligible for the transitional procedure of 37 CFR 1.129(a), and the fee set forth in 37 CFR 1.17(r) has been timely paid, the finality of the previous Office action is hereby withdrawn pursuant to 37 CFR 1.129(a). Applicant's amendment submission after final filed on March 5, 2002 has been entered.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 1-3, 6-7, and 10-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Asano et al. (U.S. 5,929,513)

Asano discloses a semiconductor device and heat sink with

(1) a semiconductor chip (36); a package body (31D) formed of a hardened encapsulant material (39); a plurality of metal leads (32), wherein each lead (32) is electrically connected to the chip (36); a flat metal plate (35) fully encapsulated within said package body (31D), wherein the chip (36) is mounted on the plate (35) and an encapsulated first portion of each of the leads (32) overhangs a periphery of the plate (35); a plurality of electrically isolated (37), encapsulated members (39); wherein each said member extends from an edge of the package body toward said plate (35) and overhangs the periphery of the plate (35); wherein said metal plate (35) is a connection with each said member (see Figure 2A);

(2) wherein the plate (35) is comprised of copper and has a CuO or CU2O film on all surfaces thereof (see column 6, lines 25-35);

(3) wherein an electrically insulative, thermally conductive adhesive layer (37) is attached between the first portion of the leads (32) and the plate (35), and said layer is covered by said encapsulant material (39) (see column 5, lines 25-26);

(6) wherein each said member extends from a corner of said package body (see Figure 2A);

(7) wherein the metal plate (35) is connected to said members by an electrically insulative, thermally conductive adhesive layer (37) (see column 5, lines 24-27);

(10) wherein the plate is formed of metal, and the metal plate has a thickness that is at least two times a thickness of said leads (see Figure 2A);

(11) wherein the encapsulant material is between said plate (35) and the first portion of the leads (32) (see Figure 2A).

Claims 30-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Asano et al. (U.S. 5,929,513)

Asano discloses a semiconductor device and heat sink with

(30) a semiconductor chip (36); a package body (31D) formed of a hardened encapsulant material (39); a plurality of metal leads (32), wherein each lead (32) is electrically connected to the chip (36); a flat metal plate (35) fully encapsulated within said package body (31D), wherein the chip (36) is mounted on the plate (35) and an encapsulated first portion of each of the leads (32) overhangs a periphery of the plate (35), and the plate has a thickness that is at least two times a thickness of the leads; and a plurality of encapsulated members (39), wherein each said member extends from

a perimeter of the package body toward the plate (35) and overhangs the periphery of the plate (35), and is in a metal to metal connection with a surface of the plate (35) (see Figure 2A);

(31) wherein an electrically insulative, thermally conductive adhesive layer (37) is attached between the first portion of the leads (32) and the plate (35), and the adhesive layer (35) is covered by the encapsulant material (39) (see column column 5, lines 24-27).

(32) wherein the encapsulant material is between said plate (35) and the first portion of the leads (32) (see Figure 2A);

(33) wherein a protrusion of the flat metal plate is stamped or swaged against the respective member, thereby forming the metal to metal connection (see column 7, lines 25-29).

Claims 21, 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asano et al. (U.S. 5,929,513) in view of Hirose (U.S. 6,117,709)

Asano teaches everything above except for the leads increase in width as those leads extend from the perimeter of the package body toward the plate. However, Hirose discloses a heat sink with first and second sides are connected to a lead frame with **(21)** wherein at least a plurality of the leads increase in width as those leads extend from the perimeter of the package body toward the plate; **(34)** wherein at least a plurality of the leads increase in width as those leads extend from the perimeter of the package body toward the plate (see columns 3 and 4, lines 51-67 and lines 1-34,

respectively. Figure 1). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the above teachings to fabricate a semiconductor device with increased thickness from the outer end toward the inner ends to enhance the contact.

Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asano et al. (U.S. 5,929,513) in view of Hirose (U.S. 6,117,709), and further view of Corisis et al. (U.S. 6,306,687 B1)

Asano and Hirose teach everything above except for said two leads defining a first slot between them, said first slot extending from the first ends of the two leads to their respective second ends. Furthermore, Corisis discloses a semiconductor integrated circuit device with **(22)** wherein two leads of increasing width are adjacent and extend from opposite sides of a first corner of the perimeter of the package body, said two leads defining a first slot between them, said first slot extending from the first ends of the two leads to their respective second ends; **(23)** further comprising a short tapered metal first member located at the first corner of the perimeter of the package body and extending into the first slot for only a portion of a length of the first slot (see columns 3 and 5, lines 43-60 and lines 39-48, respectively). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Asano, Hirose, and Corisis to manufacture a semiconductor integrated circuit device to exceed the performance criteria.

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asano et al. (U.S. 5,929,513) in view of Djennas et al. (U.S. 5,327,008)

Asano teaches the above outlined features except for three of said plurality of encapsulated members each extend diagonally from a first end located at a second corner, a third corner, and a fourth corner, respectively, of the perimeter of the package body. However, Djennas discloses a semiconductor device includes a lead frame with **(24)** wherein three of said plurality of encapsulated members each extend diagonally from a first end located at a second corner, a third corner, and a fourth corner, respectively, of the perimeter of the package body to a second end overhanging the periphery of the plate (see Figures 1 and 3). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Asano and Djennas to make a semiconductor integrated circuit device to exceed the performance criteria.

Claims 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asano et al. (U.S. 5,929,513) in view of Djennas et al. (U.S. 5,327,008), and further view of Corisis et al. (U.S. 6,306,687 B1)

Asano discloses a semiconductor device and heat sink with **(35)** a semiconductor chip (36); a package body (31D) formed of a hardened encapsulant material (39); a plurality of metal leads (32) each electrically connected to the chip (36), ...; a flat metal plate (35) fully encapsulated within said package body (31D), wherein the chip (36) is mounted on the plate (35) and an encapsulated first portion of each of the leads (32)

overhangs a periphery of the plate (35), and the plate has a thickness that is at least two times a thickness of the leads (see Figure 2A).

Asano teaches everything above except for wherein two leads of increasing width are adjacent and extend from opposite sides of a first corner of the perimeter of the package body, said two leads defining a first slot between them, said first slot extending from the first ends of the two leads to their respective second ends. However, Djennas discloses a semiconductor device includes a lead frame with **(35)**.... wherein two leads of increasing width are adjacent and extend from opposite sides of a first corner of the perimeter of the package body, and three metal pseudo tie bars each extending diagonally from a first end located at a second corner, a third corner, and a fourth corner, respectively, of the perimeter of package body to a second end overhanging the periphery of the plate and each being in a connection with the plate (see Figure 1); **(36)** wherein each pseudo tie bar includes a first portion at the second end overhanging the periphery of the plate, a second portion adjacent to the first end located at the respective corner of the perimeter of the package body, and a third portion between the second portion and the first portion, wherein the second portion is wider than the third portion and has edges that taper into the third portion (see Figure 1). Furthermore, Corisis discloses a semiconductor integrated circuit device with **(35)**..... said two leads defining a first slot between them, said first slot extending from the first ends of the two leads to their respective second ends; a metal first member located at a first corner of the package body and extending into the first slot for only a portion of a length of the first slot, the first member being encapsulated by the package

body and including intersecting straight edges that taper to a point aligned with a central axis of the first slot (see columns 3 and 5, lines 43-60 and lines 39-48, respectively). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Asano, Djennas, and Corisis to manufacture a semiconductor integrated circuit device to exceed the performance criteria.

Claim 12 is rejected under 35 U.S.C. 102(b) as being anticipated by Fogal et al. (U.S. 5,140,404)

Fogal discloses a packaged semiconductor chip with

(12) a metal frame including a central region within the frame (see Figure 3);

a plurality of metal leads extending from a first end integral with the frame to a second end adjacent to the central region, wherein at least a plurality of the leads increase in width as those leads extend from the frame toward the central region (see Figure 3);

a flat metal plate supported in the central region, wherein a first portion of each said lead overhangs a peripherery of said plate (see Figures 4, 5).

Claims 13-20, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fogal et al. (U.S. 5,140,404) in view of Asano et al. (U.S. 5,929,513)

Fogal teaches everything above except for materials of plate, adhesive layer, overhangs the periphery of the plate, extends from a corner of said frame, metal to metal contact, plate is at least twice the thickness of leads, and a protrution from a

surface of the plate. However, Asano discloses a semiconductor device and heat sink with **(13)** wherein the plate (35) is comprised of copper and has a CuO or CU2O film on all surfaces thereof (see column 6, lines 25-35);

(14) wherein an electrically insulative, thermally conductive adhesive layer (37) is attached between the first portion of the leads (32) and the plate (35) (see column 5, lines 25-26);

(16) further comprising a plurality of electrically isolated members extending from said frame adjacent to said leads; wherein each said member overhangs the periphery of the plate and is in a connection with said plate (see Figure 2A)

(17) wherein each said member extends from a corner of said package body (see Figure 2A);

(18) wherein the metal plate (35) is connected to said members by an electrically insulative, thermally conductive adhesive layer (37) (see column 5, lines 24-27);

(19) wherein each connection is a metal to metal connection between the plate and the respective member (see Figure 2A);

(20) wherein the plate is formed of metal, and the metal plate has a thickness that is at least two times a thickness of said leads (see Figure 2A);

(29) wherein each said metal to metal connection is between the respective member and a protrusion of the flat metal plate is stamped or swaged against the respective member, thereby forming the metal to metal connection (see column 7, lines 25-29).). It would have been obvious to one of ordinary skill in the art at the time of the

invention was made to combine the teachings of Fogal and Asano to fabricate a semiconductor packaging chip to meet its performance criteria.

Claims 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fogal et al. (U.S. 5,140,404) in view of Djennas et al. (U.S. 5,327,008), and further view of Corisis et al. (U.S. 6,306,687 B1)

Fogal teaches everything above except for two leads of increasing width are adjacent and extend from opposite sides of a first corner of the frame, said two leads defining an open first slot between them, said first slot extending from the first ends of the two leads to their respective second ends; further comprising a short tapered metal first member integral with the first corner of the frame and extending into the first slot for only a portion of a length of the first slot; further comprising three metal pseudo tie bars each extending diagonally from a first end integral with a second corner, a third corner, and a fourth corner, respectively, of the frame to a second end overhanging the periphery of the plate; and wherein each pseudo tie bar includes a first portion at the second end overhanging the periphery of the plate, a second portion adjacent to the first end integral with the respective corner of the frame, and a third portion between the second portion and the first portion, wherein the second portion is wider than the third portion and has edges that taper into the third portion. However, However, Djennas discloses a semiconductor device includes a lead frame with **(27)** further comprising three metal pseudo tie bars each extending diagonally from a first end integral with a second corner, a third corner, and a fourth corner, respectively, of the frame to a second

end overhanging the periphery of the plate; **(28)** wherein each pseudo tie bar includes a first portion at the second end overhanging the periphery of the plate, a second portion adjacent to the first end integral with the respective corner of the frame, and a third portion between the second portion and the first portion, wherein the second portion is wider than the third portion and has edges that taper into the third portion (see Figure 1). Furthermore, Corisis discloses a semiconductor integrated circuit device with **(25)**..... said two leads defining an open first slot between them, said first slot extending from the first ends of the two leads to their respective second ends; **(26)** further comprising a short tapered metal first member integral with the first corner of the frame and extending into the first slot for only a portion of a length of the first slot (see columns 3 and 5, lines 43-60 and lines 39-48, respectively). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Fogal, Djennas, and Corisis to manufacture a semiconductor integrated circuit device to exceed the performance criteria.

Allowable Subject Matter

Claims 37-43 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: The examiner has reviewed the prior art in light of applicant's claimed invention and finds that the claims define over the prior art. The prior art does not teach the claims combination of elements.

Response to Arguments

Applicant's arguments with respect to claims 1-3, 6-7, 10-14, and 16-36 have been considered but are moot in view of the new ground(s) of rejection.

Applicants argue that Masaki patent is not prior art and that Yoo does not diclose "said lead overhangs a periphery of said plate". However, Asano discloses a semiconductor device and heat sink (see Figure 2A) and with the combination of Fogal, Djennas, Corisis, and Hirose. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to manufacture a semiconductor integrated circuit device to exceed the performance criteria.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A Luu whose telephone number is (703)305-0129. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703)308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800